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PATENT
CASE NAME/NO.: SP03-077

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor:	J. Greg Couillard, et al.	
Serial No:	10/622,606	Group Art Unit: 2811
Filing Date:	July 18, 2003	Examiner: Thien F. Tran
Title:	SILICON CRYSTALLIZATION USING SELF-ASSEMBLED MONOLAYERS	**RESPONSE**

Commissioner for Patents
Alexandria, VA 22313-1450

RESPONSE TO EXAMINER'S RESTRICTION REQUIREMENT

In the Office Communication dated January 10, 2005, designated as Paper No. 01042005 in the above-captioned application, the Examiner issued a Restriction Requirement identifying the following groups of claims as being drawn to potentially distinct inventions:

Group I. Claims 16-24, drawn to a semiconductor device, classified in class 257, subclass 64; and

Group II. Claims 1-15, drawn to a process for making semiconductor devices, classified in class 438, subclass 22+.

Applicant elects Group II, claims 1-15 without traverse.

1. (Original) A method of fabricating a monocrystalline or polycrystalline material over a substrate, comprising:
depositing a self-assembled monolayer (SAM) over the substrate;
depositing a layer over the SAM; and
substantially crystallizing the layer.

2. (Original) A method as recited in claim 1, wherein the step of substantially crystallizing the layer further comprises annealing the substrate.

3. (Original) A method as recited in claim 2, wherein the annealing is carried out at a temperature that is less than a strain point of the substrate.

4. (Original) A method as recited in claim 1, wherein the material is a semiconductor.

5. (Original) A method as recited in claim 4, wherein the semiconductor is chosen from the group consisting essentially of: silicon, germanium and silicon-germanium.

6. (Original) A method as recited in claim 4, wherein the substrate is an oxide of the semiconductor.

7. (Original) A method as recited in claim 1, wherein the layer is an oxide.

8. (Original) A method as recited in claim 1, wherein the SAM material comprises molecules, which have an order and spacing that substantially matches an order and spacing of a lattice of the material.

9. (Original) A method as recited in claim 1, wherein the step of crystallizing the layer forms the polycrystalline the material.

10. (Original) A method as recited in claim 1, wherein the step of crystallizing the layer forms the monocrystalline material.

11. (Original) A method as recited in claim 9, wherein the polycrystalline material is polycrystalline silicon.

12. (Original) A method as recited in claim 10, wherein the crystalline material is monocrystalline silicon.

13. (Original) A method as recited in claim 9, wherein the SAM layer is a compound of R-$(CH_2)_N$-Si-R'_3, and the R' groups are cleaved during the providing of the SAM layer over the substrate.

14. (Original) A method as recited in claim 10, wherein the SAM layer is a compound of R-$(CH_2)_N$-Si-R'$_3$, and the R' group are cleaved during the depositing of the SAM layer over the substrate.

15. (Original) A method as recited in claim 2, wherein the annealing of the substrate substantially pyrolizes the SAM.

16. (Withdrawn) An apparatus, comprising:
a substrate having a monocrystalline or polycrystalline material disposed thereover, wherein the substrate has a strain point that is lower than a forming temperature of the polycrystalline or monocrystalline material.

17. (Withdrawn) An apparatus as recited in claim 16, wherein the apparatus is a display device.

18. (Withdrawn) An apparatus as recited in claim 16, wherein the material is a semiconductor.

19. (Withdrawn) An apparatus as recited in claim 17, wherein the display device is chosen from the group consisting of flat panel displays (FPD's) displays.

20. (Withdrawn) An apparatus as recited in claim 18, wherein the semiconductor is chosen from the group consisting essentially of: silicon, germanium and silicon-germanium.

21. (Withdrawn) An apparatus as recited in claim 18, wherein the carriers of the semiconductor material have a mobility in the range of approximately 50 cm^2/Vsec to approximately 600 cm^2/Vsec.

22. (Withdrawn) An apparatus as recited in claim 18, wherein at least one electronic device is formed of the semiconductor.

22. (Withdrawn) An apparatus as recited in claim 21, wherein the mobility has a uniformity on the order of approximately ±10%.

23. (Withdrawn) An apparatus as recited in claim 16, wherein grains of the material have a preferred orientation.

24. (Withdrawn) An apparatus as recited in claim 16, wherein the material is polycrystalline silicon having grain sizes of approximately 1 μm to approximately 2 μm.

Applicants believe that no extension of time is necessary to make this Response timely. Should Applicants be in error, Applicants respectfully request the Office grant such time extension pursuant to 37 C.F.R. § 1.136(a) as necessary to make this Response timely, and hereby authorizes the Office to charge any necessary fee or surcharge with respect to said time extension to the deposit account of the undersigned firm of attorneys, Deposit Account 03-3325.

Please direct any questions or comments to Thomas R. Beall at (607) 974-3921.

Respectfully submitted,

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Date: January 20, 2005

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CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8: I hereby certify that this paper and any papers referred to herein are being deposited with the U.S. Postal Service, as first class mail, postage prepaid, addressed to Commissioner of Patents, Alexandria, VA 22313-1450 on January 20, 2005.

Thomas R. Beall